Hybrid Power Analysis Approach for Electronic System Design

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Abstract-The power estimation in electronic system designs (ESD) has become a significant problem. To keep a balanced approach between the estimation accuracy and speed is the key challenge in the system design. In this paper we present a power analysis method at high abstraction level. We focus on the statistically power dissipation sources of the individual ESD blocks and interconnects/buses of the system. Our hybrid technique combines the regression analysis and look-up-table (LUT) approaches with the non-linear behavioral function. Our algorithm generates input binary signals with five statistical characteristics that help to estimate the average power dissipation. For the power function, we performed Monte-Carlo zero-delay simulation and observed the exact steady-state power behavior of the system. Our power model estimates an accurate power with 10.16% average error. The results are compared with a commercial power estimation tool for the validity of our proposed approach.

Keywords-Low-power, Power estimation, Look-up-table, Register transfer level, CAD/EDA tools

I. INTRODUCTION

Low-Power consumption in electronic system design is becoming an important issue that cannot be ignored. Its flow gives designer a powerful methodology to optimize, estimate and analyze today's increasing power concerns. The rapid growth of transistor density in ESD have made power an important design constraint. At deep submicron level, the reduction of cooling may be the significant factor of integrated circuit (IC) process. ESD is another motivation to investigate the low-power-based system. Power optimization and estimation has nowadays become a difficult task for which the conventional approaches often prove to be inadequate. A key objective in low-power systems is accurate and fast power analysis. Power estimation at high design abstraction level gives new solutions to efficient power problems. Hence, power estimation and optimization approach for low-power is the challenge to a successful design. In order to handle power, commercial electronic design automation (EDA) tools help the designers in the initial stages of the system design procedures. These tools are useful for minimizing the power dissipation in ESD system. Early power analysis ignores the lengthy procedure to redesign and handles the power budget during the design cycles in the later stages.

As rapid growth of system's complexity and verifications become increasingly difficult and time consuming, power and performance analysis of the design flow are essential for shortening the turn-around time. The design cost and time-to-market of the electronic systems can be greatly reduced through the reuse of predesigned circuits. Power methodology further supports reuse design in a plug-and-play fashion, including buses and hierarchical interconnection infrastructure. Reuse design techniques employing ESD cores cut down on time-to-market, and fast estimation shortens the design evaluation time, which is more efficiently used in design-space exploration. At the initial stage of the pre-design phase, the designers tried to find the possibility of the design exploration space and the power, area, speed requirements. Lot of work has been presented in the past to estimate power of electronic systems at different abstraction levels.

II. LITERATURE REVIEW

A good review of the most effective approaches at different level of the design can be found in [i, ii]. Power analysis models at high-level can be categorized as: linear regression-based, LUT-based or hybrid-based. Regression models estimate power of the individual component with a compact form but it do not deal with the non-linear behavior. Register-transfer level (RTL) cycle accurate model was presented in [iii] to handle with the non-linear behavior with the piecewise regression approach. The improved work of [iii] was further proposed with the automated regression modeling [iv].

LUT-based technique is the most popular approach in the power analysis procedure. Several commercial EDA tools are widely used LUT approach for handling power consumption of each logic block. The impact of the LUT size in the power estimation was discussed in [v]. If the LUT size decreases, then the estimation error increases exponentially. The extended work was

presented in [vi] to include more independent variables in the model to improve error in the expense of the LUT size.

Hybrid model includes both concepts of regression and LUT approaches. Recently, [vii] demonstrated an efficient hybrid method for the power analysis to minimize the length of the simulation with different levels of the granularity. Such approach uses selectively chooses blocks according to its relative power dissipation to the overall power performance. If it does not effectively influence of the system's power consumption, it may be ignored with some error.

In this work, the two separate hybrid power macro-models are developed for the power estimation of the ESD. These models estimate power for different ESD blocks/buses in the system. These models are only dependent on the environment where blocks and buses are being used. The input signals investigate the accurate power in electronic system. These signals influence the power consumption of ESD blocks and buses in the design. The model uses the average input statistical characteristics for ESD *blocks* are the transition-density *'TD'*, the signal-probability *'SP',* and the spatio-temporal correlation *'ST_C'*. The average input statistical characteristics of *buses* are the self and coupling transition densities 'S_{TD}, C_{TD}' respectively. These characteristics are used in two separate power models in experiments and achieve comparatively good accuracy. The target is the accurate average total power consumption of a hierarchical blocks and buses under a user-specified application input waveforms.

The paper is organized as follows. In Section III, the detailed background of hybrid power analysis methodology is discussed. In Section IV, the results and discussion is demonstrated. Finally, the Section V summarizes the work.

III. Power Estimation Method

One of the most challenging aspects in the construction of a power macro-model is the choice of the model's characteristics. These characteristics should capture the features that are primarily responsible for a system's dissipation and can thus help in obtaining good estimates of its power dissipation. The flow of high-level power estimation methodology is shown in Fig. 1. The approach consists of the following steps:

1. Characterization of each ESD block/bus at the high-level design library by simulating it under pseudo random signals and fit statistical variables regression curve to the power dissipation results using a least-mean-square (LMS) error fit.
2. Extractions of the power function from parameter model for blocks *'TD, SP, ST_C'* and for buses 'S_{TD}, C_{TD}' using Monte-Carlo simulation approach. The high-level simulator collects the power values for various blocks/buses in the ESD System.
2. Evaluation of the power model function for block/bus design. These are found in the library by plugging the parameter values in the corresponding model function.

A. Linear Regression Analysis

The proposed hybrid model is the combination of linear regression and LUT approaches. To obtain power model, a linear function in (1) estimates power of the given input signals.

$$P_{Block\_avg} = \beta_0 + \beta_1.\alpha_1 + ... + \beta_{n-1}.\alpha_{n-1} + \beta_n.\alpha_n + \varepsilon \quad (1)$$

where 'P_{Block_avg}' is the average power dissipation of the individual ESD block, '$\beta_0, \beta_1, ...\beta_{n-1}, \beta_n$' are the regression coefficients obtained from the regression analysis, '$\alpha_0, \alpha_1, ...\alpha_{n-1}, \alpha_n$' are the statistical characteristics of each input and ε is the error. The parameters of the regression are determined using the linear regression by finding the least-square fit. Equation (1) can be expressed in (2):

$$P_{IP\_avg} = \beta_0 + \beta_1.TD + \beta_2.SP + \beta_3.SC + \beta_4.TC + \varepsilon \quad (2)$$

where *'TD, SP, SC, TC'* are the statistical characteristics of our model.

The regression equation in (2) can be computed by applying the set defined input pattern values of *'TD, SP, SC,* and *TC'*. The determination coefficient p^2 is measured to improve the quality of (2). It measures the proportionality of data set patterns of the input characteristics that helps to predict the accurate power. p^2 varies from 0 to1 and it is defined in (3):

$$p^2 = 1 - \frac{\varepsilon_s}{r} \quad (3)$$

where ε and r is defined in (4) and (5):

$$\varepsilon_s = \sum \left(x_i - y_i\right)^2 \quad (4)$$

$$r = \sum \left(x_i - \bar{x}\right)^2 \quad (5)$$

with $\bar{x}$ is the mean of the estimated data, x_i predicts the values and y_i is the data set value.

B. LUT-Based Power Estimation for ESD blocks

The power model characteristics are defined in [viii, ix]. We propose an input signal generation algorithm which generates test stimuli with *'TD, SP, ST_C'*. The LUT-based power model estimates the average power dissipation of each ESD block in (6).

$$P_{Block\_avg} = f(TD, SP, ST\_C) \quad (6)$$

For the given block with the primary inputs width *'w'* and the input binary signals length *'l'* in (7):

$$l = \{(l_{11}, l_{12}, \ldots, l_{1w}), (l_{21}, l_{22}, \ldots, l_{2w}), \ldots (l_{n1}, l_{n2}, \ldots, l_{nw})\} \quad (7)$$

The *f(.)* in (6) is the input pattern dependent, so the length and the width in the pattern generation are dependent on the number of primary inputs of the individual block. In most cases, the *'TD'* and *'SP'* have effective role in the power dissipation due to their characteristics of transition activities of input signals in any digital system. In observations, the correlation factor *'ST_C'* is normally dependent on the number of primary inputs and the size (number of gates) of the individual block. Further, in case of '*ST_C'*, if *'w'* increases then spatial-correlation '*SC'* are more effective than temporal-correlation '*TC'* Similarly, in case of increases *'l'*, the *'TC'* is more significant than the *'SC'* in any input pattern. Hence equation (6) is further modified and introduced two sub-functions in (8) and (9).

$$P_{Block\_A\_avg} = f(TD, SP, SC_{\rightarrow w}) \quad (8)$$

$$P_{Block\_B\_avg} = f(TD, SP, TC_{\rightarrow l}) \quad (9)$$

where '$SC_{\rightarrow w}$' and '$TC_{\rightarrow l}$' are the width and length dependent correlation characteristics.

B. LUT-Based Power Estimation for Buses

In the earlier literature, extensive power modeling approaches of interconnects/buses have been introduced [x, xi]. Our LUT-based power model estimates the average power dissipation of interconnects in (10).

$$P_{Interconnect\_avg} = f(S_{TD}, C_{TD}) \quad (10)$$

where 'S_{TD}' and 'C_{TD}' are the self and coupling transition densities of interconnects. The 'C_{TD}' depends on the activity between the two adjacent interconnects.

The *f(.)* in (10) is the input pattern dependent. The input signal generator generates patterns according to the number of interconnects of the individual bus. The *f(.)* is a mapping-method to be performed during the characterization of the two transition densities. To find function *f(.)*, we must sample a set number of streams with several 'S_{TD}, C_{TD}' values. The application of the power estimation on each interconnect requires knowledge of the signal characteristics among interconnects. To find an average power dissipation of the local or global shared bus 'P_{Bus_avg}' depending on the number of interconnects (in the system) can be computed in (11) using (10).

$$P_{Bus\_avg} = f(S_{TD\_Bus}, C_{TD\_Bus}) \quad (11)$$

where 'S_{TD_Bus}' and 'C_{TD_Bus}' are the self and coupling transition densities of bus defined in (12), (13):

$$S_{TD\_Bus} = \sum_{i=1}^{n} S_{TD_i} \quad (12)$$

$$C_{TD\_Bus} = \sum_{i=1}^{n-1} S_{TD_{i,i+1}} \quad (13)$$

Here *n* is the number of interconnects of the bus.

D. Hybrid Power Estimation for ESD

The total power consumption of a system is obtained by adding all its dissipative components. The *f(.)* in (6), (8), (9), (10) and (11) is a mapping-method to be performed during the characterization of the input signals. To find function *f(.)*, a set pattern of these signals with several values of *'TD, SP, ST_C'* and 'S_{TD}, C_{TD}'. The application of the power estimation on each block requires knowledge of the input signal characteristics among individual blocks. The total average power dissipation of the ESD system 'P_{ESD_System}' is extracted in (14) using (8), (9) and (11).

$$P_{ESD\_System} = \sum_{i=1}^{n} P_{iBlock\_avg} + \sum_{i=1}^{n} P_{iBus\_avg} \quad (14)$$

Monte-Carlo zero-delay simulation technique [ix] is used with several sequences of their input signal characteristics given to the ESD block and the power dissipation is estimated to the each sample of the input signals. These power samples are needed to determine whether the entire process is necessary to repeat and full-fill the given criteria. The estimation must satisfy the top-level circuit under the user-specified confidence and error levels. Our power estimation strategy is to sums up the estimates to produce total average power by the macro-model function in (14). The interpolation-scheme [xii] may be performed if the input characteristics do not match their statistics.

IV. Results & Discussion

To validate hybrid power estimation method, the experimental work is evaluated on ESD system as shown in Fig 1. The figure has *n* umber of blocks with different sizes. These blocks are connected with each other through the local and global buses to construct the overall ESD system. The model uses a nonlinear function in (14) to estimate the average power dissipation.

In power estimation procedure, the sequence of an

input pattern is generated for the desired input characteristics '*TD*, *SP*, *ST_C*' and 'S_{TD}, C_{TD}' for ESD blocks and buses respectively. Then using LUT technique, the functional simulations are performed with RTL power simulator and the average power dissipation is extracted by the output waveforms of the individual ESD block or bus. At this stage, the power functions in (6), (8), (9), (10) and (14) can be defined.

This power estimation procedure is divided into two phases: In the first phase, we generate random digital input signals according to the statistical characteristics with the specified probabilistic range between [0-1] for the given block/bus and the average power consumption is estimated using power

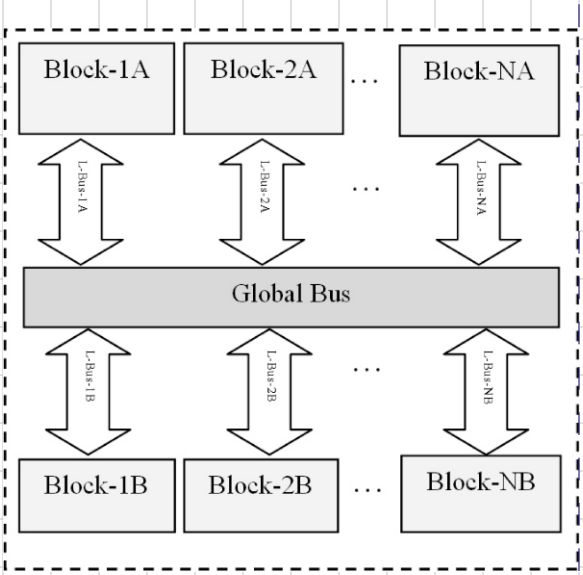

Fig. 1. Example of ESD architecture

function *f(.)* in (6) or (11). These functions map the input characteristics of each block/bus. In the second phase, a Monte-Carlo zero-delay simulation is performed with several input signals of their statistical properties, whereas the least square fitting is performed for linear regression analysis to find the quality of the power functions P_{Block_avg} and P_{Bus_avg}. Several values are determined by LUT-based approach. Then we estimate the average power results. The accuracy of our power macro-model is tested by running gate-level and RTL simulations. We compare our power results with Xilinx and HSPICE commercial tools. At the end, we compute errors to find the accuracy of our model.

In our preliminary work with ESD system, the hybrid technique intends to reduce larges simulations at RTL. Our method allows fast power estimation by a simple addition of all blocks and buses. The average power dissipation of ESD system 'P_{ESD_System}' is extracted using (14). The main advantage of our hybrid method is that it can provide fast and accurate estimates; thus, it helps designers to explore different complex blocks in real time. We opted for a simple functions with low-order polynomial dependency on *f(.)* in (6), (8), (9), and (11). We compare our estimated power with simulated power estimation (taken from the power simulator) using (15) and (16) to evaluate the accuracy of our power estimation function. The maximum, minimum, average and root mean square (rms) errors are computed.

In our experiments, we used ESD blocks with different sizes shown in Table 1. Each block may be considered as a single block in a medium VLSI chip. The sizes of our larger blocks are close enough in today's embedded electronic circuits. Hence our power estimation strategy is consistent with individual block-by-block for input pattern generation. The randomly generated sequences have relatively accurate statistics. Our pattern generator can generate a set number of sequences over the entire space range. Therefore, it enables us to perform extensive experiments to reveal the relation between ESD design power dissipation and specific statistics of the input signals. In our study, we used different blocks/buses and for individual block/bus, we generated 400 to 1900 sequences with '*TD*, *SP*, *ST_C*' and 'S_{TD}, C_{TD}' evenly distributed in the three/two dimensional space. Our parameters granularity is 0.2 over the entire space. In practice, much larger sequences should be used for larger circuits. Roughly speaking, for a given block/bus, we empirically observe that sufficiently long input sequences that produce similar steady-state power exhibit similar total power. Given block/bus, for all the input sequences that produce a steady-state power, we believe that hazardous power corresponding to an input sequences have the behavior of a random variable. Furthermore, among all these input sequences that produce a steady-state power, longer sequences tend to have smaller variance than shorter sequences. For the verification of our random sequences, we compared our power results with the functional sequences power results and found a 96% correlation. Synthetic validation is performed by applying a uniform set of stochastically generated test-benches. All the results to be presented were performed with a 3% error-tolerance ($\varepsilon = 0.07$) and 98% confidence ($\alpha = 0.03$). Table I and Table II, illustrates the set number of the input vectors and the average relative errors of the estimate values obtained with our macro-model function. For the input characteristics, '*TD*, *SP*, *ST_C*, and 'S_{TD}, C_{TD}' the specified range between [0-1]. The function is more accurate estimating the average power in some cases than others. For example in figure 2, the given input values are more accurate for specifying the range of region between [0.25-0.75] and less accurate of region between [0-0.25] and [0.75-1].

It is evident from Table 1 that the model function *f(.)* is accurate for estimating the average power for digital block. In Table 1, the first column shows the name of the block. The three dimensional input model estimates the average 6.08%

TABLE I
ACCURACY OF POWER ESTIMATES FOR INDIVIDUAL BLOCK

Core	$\%\varepsilon_{min}$	$\%\varepsilon_{max}$	$\%\varepsilon_{avg}$	$\%\varepsilon_{rms}$	# gates
Blk-1A	11.20	13.12	11.83	11.78	885
Blk-2A	3.25	4.32	3.56	3.38	463
Blk-3A	14.32	15.30	14.79	14.61	921
Blk-4A	5.14	6.92	5.65	5.54	310
Blk-5A	4.54	6.42	5.56	5.33	456
Blk-6A	7.30	9.35	8.52	8.39	843
Blk-7A	8.23	9.90	8.76	8.64	760
Blk-8A	4.56	6.03	5.67	5.78	658
Blk-1B	6.43	8.12	7.52	7.80	810
Blk-2B	9.12	10.59	9.81	9.93	830
Blk-3B	2.17	3.37	2.84	2.74	420
Blk-4B	4.76	6.16	5.53	5.68	667
Blk-5B	5.57	6.35	5.98	5.86	323
Blk-6B	5.02	6.91	6.04	6.18	644
Blk-7B	1.34	3.07	2.62	2.78	1190
Blk-8B	4.34	5.93	4.94	4.56	944
$\%\varepsilon_{avg}$	**6.08**	**7.62**	**6.85**	**6.80**	**695**

TABLE II
ACCURACY OF POWER ESTIMATES OF BUSES

Bus	$\%\varepsilon_{min}$	$\%\varepsilon_{max}$	$\%\varepsilon_{avg}$	$\%\varepsilon_{rms}$	# lines
L-Bus-1A	6.24	8.38	7.45	7.65	16
L-Bus-2A	5.53	7.24	6.25	6.02	16
L-Bus-3A	6.23	8.24	7.19	7.03	16
L-Bus-4A	9.56	11.43	12.01	12.09	16
L-Bus-5A	5.30	7.03	6.49	6.29	8
L-Bus-6A	4.90	6.12	5.37	5.93	8
L-Bus-7A	5.41	6.98	6.38	6.45	8
L-Bus-8A	6.47	7.86	7.16	7.43	8
L-Bus-1B	2.84	3.97	3.21	3.64	16
L-Bus-2B	7.94	10.29	9.01	9.87	16
L-Bus-3B	5.37	8.13	6.35	6.41	16
L-Bus-4B	3.83	5.48	4.46	4.37	16
L-Bus-5B	4.48	6.39	5.49	5.06	8
L-Bus-6B	5.83	7.17	6.57	6.07	8
L-Bus-7B	2.69	4.98	3.15	3.61	8
L-Bus-8B	1.92	3.05	2.69	2.18	8
G-Bus-1	10.54	17.22	14.50	14.44	24
$\%\varepsilon_{avg}$	**5.59**	**7.64**	**6.69**	**6.77**	**12.71**

minimum, 7.62% maximum, 6.85% average and 6.80% rms relative errors are demonstrates in columns two, three, four, and five respectively. Columns six gives the number of logic gates of each core consists of 300-1200 logic gates in the ESD system. Our macro-model separately estimates the power consumption of interconnects/buses among different blocks. In Table 2, the first column shows the name of the local or global bus. The two dimensional input macro-model estimates the average 5.59% minimum, 7.64% maximum, 6.69% average and 6.77 rms relative errors are demonstrates in columns two, three, four, and five respectively.. Columns six gives the number of lines/interconnects in each bus consists of 8-24 bits in the ESD system. Figure 2 plots the variation of the power values with the trial interval length (clock cycle) and it demonstrates the length is 1000 for one of the four blocks in the system. The warm-up length is about 400, while the vertical line represents the steady-state value at 800.

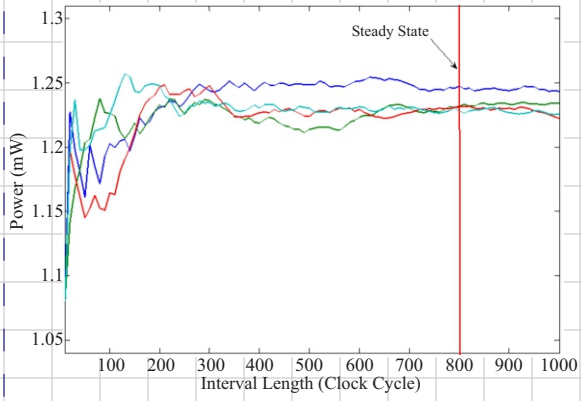

Fig. 2. Power changes with sequence length for different blocks in ESD System

The above results demonstrate that our technique can be implemented to achieve fast and accurate power estimation in the early stage of any ESD design. The average power dissipation of ESD system 'P_{ESD_System}' is extracted using (14) by a simple addition of all digital blocks and buses. In our experiments, the average error of the entire system is 10.16%. This error may be reduced by using different optimization techniques to improve the power dissipation of the system. One important source of error is due to delay elements such as glitch activities, jitter, skew and other power dissipative elements. In this paper we do not consider these factors and assume zero-delay model approach.

V. CONCLUSION

We have demonstrated a zero-delay power estimation technique at high-level applied to ESD system. In our preliminary work, we extracted two different statistical models to estimate power dissipation for individual blocks and bus in the design. For an entire ESD system, the average power is extracted by a simple addition of all power estimation results of these two models. In our experiments, we measured 10.16% of the average error in the entire system. This error may be reduced by using different optimization techniques to handle the power

dissipative elements such as glitch activities, jitters, skews and other factors. Currently, we are evaluating our approach for more complex ESD systems and are working to further improve its accuracy.

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